IT IS CLAIMED:

1. In a non-volatile memory having an array of memory storage units, each unit having a charge storage unit between a control gate and a channel region defined by a source and a drain, and a bit line switchably coupled to the drain, a method of programming a page of contiguous memory storage units having interconnected control gates to their target states, comprising:

(a) providing a bit line switchably coupled to the drain of each memory storage unit and a word line coupled to all the control gates of said page of memory storage unit;

(b) applying an initial, first predetermined voltage to the bit lines of designated memory storage units of the page to enable programming;

(c) applying an initial, second predetermined voltage to the bit lines of un-designated memory storage units of said page to be program inhibited;

(d) floating the program-enabled bit lines, while raising the program-inhibited bit lines from said second predetermined voltage by a predetermined voltage difference to a third predetermined voltage, wherein a predetermined portion of the predetermined voltage difference is coupled as an offset to any neighboring, floated, program-enabled bit lines, and said third predetermined voltage enables floating of the channel of each program-inhibited memory storage unit;

(e) applying a programming voltage pulse to the word line in order to program the designated memory storage units of the page, wherein those un-designated memory storage units of the page are program- inhibited by virtue of their floated channel boosted to a program inhibited voltage condition, and a perturbation resulted from the boosting on any neighboring program-enabled memory storage units is compensated by said offset.

2. The method as in claim 1, further comprising:

(f) verifying the selected memory storage units under programming;

(g) re-designating any memory storage units that have not been verified; and

(h) repeating (c) to (g) until all of said page of memory storage units have been verified.

3. The method as in any one of claims 1 or 2, wherein said floating the program-enabled bit lines precedes the floating of the channel of each program-inhibited memory storage unit.

4. The method as in any one of claims 1 or 2, wherein said floating the program-enabled bit lines is after the floating of the channel of each program-inhibited memory storage unit.

5. The method as in any one of claims 1 or 2, wherein said page of memory storage units forms a row of said array.

6. The method as in any one of claims 1 or 2, wherein said page of memory storage units forms a segment of a row of said array.

7. The method as in any one of claims 1 or 2, wherein:

said memory is organized as an array of NAND chains of memory storage units, each chain having a plurality of memory storage units connected in series, and said page of memory storage units is constituted from a memory storage unit from each NAND chain among a page thereof.

8. The method as in any one of claims 1 or 2, wherein each memory storage unit stores one bit of information.

9. The method as in any one of claims 1 or 2, wherein each memory storage unit stores more than one bit of information.

10. The method as in any one of claims 1 or 2, wherein said charge storage unit is a floating gate.

11. The method as in any one of claims 1 or 2, wherein said charge storage unit is a dielectric layer.

12. The method as in any one of claims 1 or 2, wherein said non-volatile memory is in the form of a card.

13. The method as in any one of claims 1 or 2, further comprising:

setting a program-enabled bit line to a predetermined potential that substantially maximizes programming efficiency whenever it has two neighboring bit lines that are also program-enabled.

14. The method as in any one of claim13, wherein said predetermined potential is at ground.

15. In a non-volatile memory having an array of memory storage units, each unit having a charge storage unit between a control gate and a channel region defined by a

source and a drain, and a bit line switchably coupled to the drain, a programming circuit for programming a page of contiguous memory storage units having interconnected control gates to their target states comprising:

a bit line switchably coupled to the drain of each memory storage unit;

a word line coupled to all the control gates of said page of memory storage unit;

means for applying an initial, first predetermined voltage to the bit lines of designated memory storage units of the page to enable programming;

means for applying an initial, second predetermined voltage to the bit lines of un-designated memory storage units of said page to be program inhibited;

means for floating the program-enabled bit lines, while raising the program-inhibited bit lines from said second predetermined voltage by a predetermined voltage difference to a third predetermined voltage, wherein a predetermined portion of the predetermined voltage difference is coupled as an offset to any neighboring, floated, program-enabled bit lines, and said third predetermined voltage enables floating of the channel of each program-inhibited memory storage unit;

means for applying a programming voltage pulse to the word line in order to program the designated memory storage units of the page, wherein those un-designated memory storage units of the page are program- inhibited by virtue of their floated channel boosted to a program inhibited voltage condition, and a perturbation resulted from the boosting on any neighboring program-enabled memory storage units is compensated by said offset.

16. The non-volatile memory as in claim 15, further comprising:

means for setting a program-enabled bit line to a predetermined potential that substantially maximizes programming efficiency whenever it has two neighboring bit lines that are also program-enabled.

17. The non-volatile memory as in claim 16, wherein said predetermined potential is at ground.

18. In a non-volatile memory having an array of memory storage units, each unit having a charge storage unit between a control gate and a channel region defined by a source and a drain, and a bit line switchably coupled to the drain, a programming circuit for programming a page of contiguous memory storage units having interconnected control gates to their target states comprising:

a bit line switchably coupled to the drain of each memory storage unit;

a word line coupled to all the control gates of said page of memory storage unit;

a controller and a power supply responsive to said controller;

said controller designating memory storage units to be programmed among said page;

said power supply applying a first predetermined voltage to the bit lines of the designated memory storage units of said page to enable programming;

said power supply applying a second predetermined voltage to the bit lines of un-designated memory storage unit of said page to be program inhibited;

switches responsive to said controller for floating the program-enabled bit lines while said power supply raising the program-inhibit bit lines from said second predetermined voltage by a predetermined voltage difference to a third predetermined voltage, wherein a predetermined portion of said predetermined voltage difference is coupled as an offset to any neighboring, floated, program-enabled bit lines, and said third predetermined voltage enables floating of the channel of each program-inhibited memory storage units; and

said power supply a programming voltage pulse to the word line in order to program the designated memory storage units of the page, wherein those un-designated memory storage units of the page are program- inhibited by virtue of their floated channel boosted to a program inhibited voltage condition, and a perturbation resulted from the boosting on any neighboring program-enabled memory storage units is compensated by said offset.

19. The non-volatile memory as in claim 18, wherein said floating the program-enabled bit lines precedes the floating of the channel of each program-inhibited memory storage unit.

20. The non-volatile memory as in claim 18, wherein said floating the program-enabled bit lines is after the floating of the channel of each program-inhibited memory storage unit.

21. The non-volatile memory as in claim 18, wherein said page of memory storage units forms a row of said array.

22. The non-volatile memory as in claim 18, wherein said page of memory storage units forms a segment of a row of said array.

23. The non-volatile memory as in claim 18, wherein:

said memory is organized as an array of NAND chains of memory storage units, each chain having a plurality of memory storage units connected in series, and said page of memory storage units is constituted from a memory storage unit from each NAND chain among a page thereof.

24. The non-volatile memory as in claim 18, wherein each memory storage unit stores one bit of information.

25. The non-volatile memory as in claim 18, wherein each memory storage unit stores more than one bit of information.

26. The non-volatile memory as in claim 18, wherein said charge storage unit is a floating gate.

27. The non-volatile memory as in claim 18, wherein said charge storage unit is a dielectric layer.

28. The non-volatile memory as in claim 18, wherein said non-volatile memory is in the form of a card

29. The non-volatile memory as in claim 18, wherein each of said memory storage units to be programmed is connectable to a bit line, and said not-volatile memory further comprising:

a voltage source for setting said bit line to a predetermined potential that substantially maximizes programming efficiency whenever it has two adjacent bit lines associated with neighboring memory storage units not inhibited for programming.

30. The non-volatile memory as in claim 16, wherein said predetermined potential is at ground.